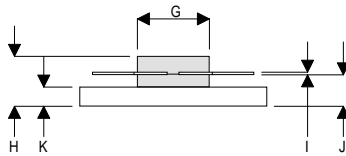
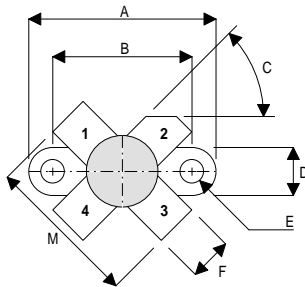


MECHANICAL DATA



DA

PIN 1 SOURCE                      PIN 2 DRAIN  
 PIN 3 SOURCE                      PIN 4 GATE

DIM	mm	Tol.	Inches	Tol.
A	24.76	0.13	0.975	0.005
B	18.42	0.13	0.725	0.005
C	45°	5°	45°	5°
D	6.35	0.13	0.25	0.005
E	3.17	0.13	0.125 DIA	0.005
F	5.71	0.13	0.225	0.005
G	9.52	0.13	0.375	0.005
H	6.60	REF	0.260	REF
I	0.13	0.02	0.005	0.001
J	4.32	0.13	0.170	0.005
K	2.54	0.13	0.100	0.005
M	20.32	0.25	0.800	0.010

**GOLD METALLISED  
 MULTI-PURPOSE SILICON  
 DMOS RF FET  
 20W – 50V – 175MHz  
 SINGLE ENDED**

**FEATURES**

- SIMPLIFIED AMPLIFIER DESIGN
- SUITABLE FOR BROAD BAND APPLICATIONS
- LOW  $C_{rss}$
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN – 16 dB MINIMUM

**APPLICATIONS**

- HF/VHF COMMUNICATIONS  
 from 1 MHz to 175 MHz

**ABSOLUTE MAXIMUM RATINGS** ( $T_{case} = 25^{\circ}C$  unless otherwise stated)

$P_D$	Power Dissipation	50W
$BV_{DSS}$	Drain – Source Breakdown Voltage	125V
$BV_{GSS}$	Gate – Source Breakdown Voltage	$\pm 20V$
$I_{D(sat)}$	Drain Current	3A
$T_{stg}$	Storage Temperature	-65 to 150°C
$T_j$	Maximum Operating Junction Temperature	200°C

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## ELECTRICAL CHARACTERISTICS (T<sub>case</sub> = 25°C unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
B <sub>V</sub> DSS Drain–Source Breakdown Voltage	V <sub>GS</sub> = 0      I <sub>D</sub> = 100mA	125			V
I <sub>DSS</sub> Zero Gate Voltage Drain Current	V <sub>DS</sub> = 50V      V <sub>GS</sub> = 0			1	mA
I <sub>GSS</sub> Gate Leakage Current	V <sub>GS</sub> = 20V      V <sub>DS</sub> = 0			1	μA
V <sub>GS(th)</sub> Gate Threshold Voltage*	I <sub>D</sub> = 10mA      V <sub>DS</sub> = V <sub>GS</sub>	1		7	V
g <sub>fs</sub> Forward Transconductance*	V <sub>DS</sub> = 10V      I <sub>D</sub> = 0.5A	0.8			S
G <sub>PS</sub> Common Source Power Gain	P <sub>O</sub> = 20W	16			dB
η Drain Efficiency	V <sub>DS</sub> = 50V      I <sub>DQ</sub> = 0.1A	50			%
VSWR Load Mismatch Tolerance	f = 175MHz	20:1			—
C <sub>iss</sub> Input Capacitance	V <sub>DS</sub> = 50V      V <sub>GS</sub> = -5V      f = 1MHz			60	pF
C <sub>oss</sub> Output Capacitance	V <sub>DS</sub> = 50V      V <sub>GS</sub> = 0      f = 1MHz			25	pF
C <sub>rss</sub> Reverse Transfer Capacitance	V <sub>DS</sub> = 50V      V <sub>GS</sub> = 0      f = 1MHz			1.5	pF

\* Pulse Test:    Pulse Duration = 300 μs , Duty Cycle ≤ 2%

## HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area.

**THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.**

## THERMAL DATA

R <sub>THj-case</sub>	Thermal Resistance Junction – Case	Max. 3.5°C / W
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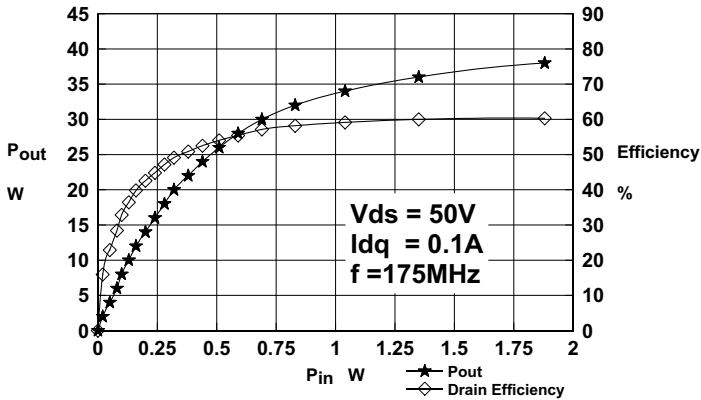


Figure 1

Power Output and Efficiency vs. Power input

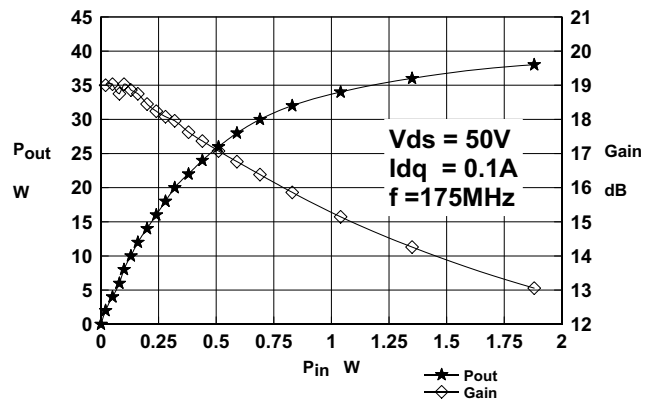


Figure 2

Power Output and Gain vs Power Input

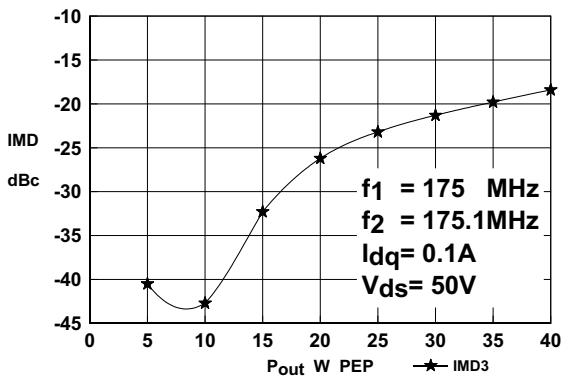


Figure 3

IMD3 vs Power Output

OPTIMUM SOURCE AND LOAD IMPEDANCE

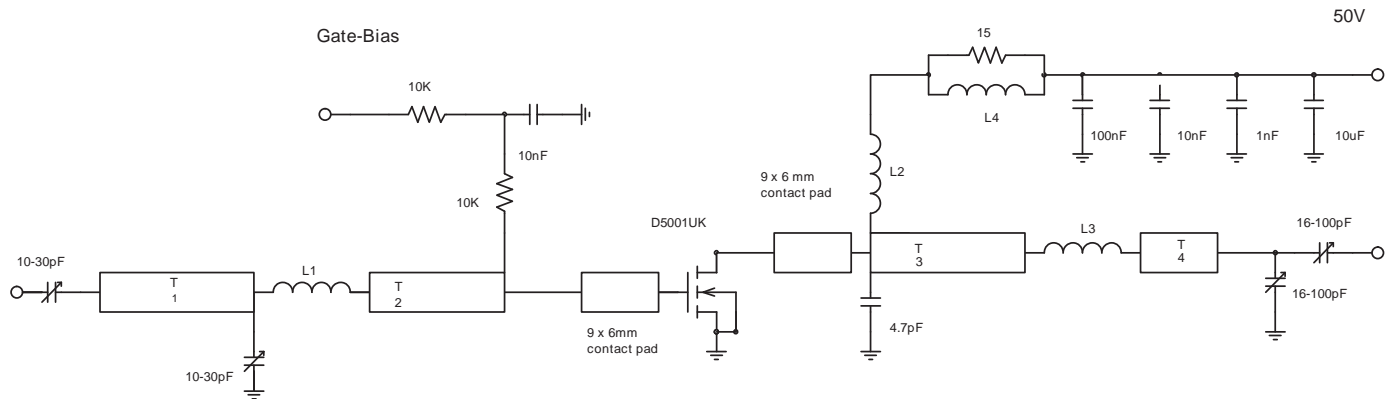
Frequency MHz	Z <sub>S</sub> Ω	Z <sub>L</sub> Ω
175	9.5 + j14.1	12.3 + j10.2

Typical S Parameters

! Vds=50V Idq=0.1A  
 # MHZ S MA R 50

!Freq !Mhz	S11		S21		S12		S22	
	mag	ang	mag	ang	mag	ang	mag	ang
30	0.85	-108.7	9.765	172.5	0.018	69.9	0.726	-69.2
40	0.846	-109.8	9.588	163.6	0.019	65.8	0.718	-70.1
50	0.84	-111.2	9.473	154.9	0.019	60.2	0.709	-71.2
60	0.837	-113.1	8.991	146.1	0.02	55.2	0.699	-72.6
70	0.835	-116	8.521	139.2	0.021	50.7	0.689	-74.4
80	0.833	-118	8.104	134.4	0.022	47.6	0.678	-78.1
90	0.831	-120	7.662	127.9	0.023	44.6	0.673	-80.6
100	0.829	-123.3	7.304	122.9	0.023	42.7	0.671	-83.6
110	0.828	-125.2	6.991	117.8	0.023	40.5	0.671	-85.3
120	0.825	-127.4	6.732	114.6	0.023	40.2	0.669	-87.9
130	0.823	-130	6.406	109.6	0.023	39.8	0.665	-88.6
140	0.82	-131.9	6.155	105	0.022	39.9	0.664	-89.6
150	0.816	-135	5.868	100.7	0.021	40.6	0.663	-91.4
160	0.81	-137.6	5.644	96.3	0.021	41.9	0.664	-92.6
170	0.807	-139.8	5.305	91.2	0.02	44.2	0.665	-94.2
180	0.803	-142.8	4.989	87.4	0.019	48	0.665	-96.8
190	0.804	-144.7	4.656	83.5	0.019	52	0.667	-98.6
200	0.806	-147.3	4.402	81.1	0.019	57.2	0.671	-101.2
210	0.803	-149.2	4.09	79.8	0.019	62.2	0.672	-103
220	0.808	-151.5	3.989	78.7	0.02	68.2	0.671	-103.5
230	0.802	-153.1	3.859	76.5	0.02	71.6	0.677	-105.6
240	0.807	-155.2	3.717	74	0.021	76.1	0.685	-107.9
250	0.811	-156.7	3.57	71.3	0.022	79.4	0.687	-109.9
260	0.812	-158.9	3.435	68.4	0.023	84.1	0.698	-111.9
270	0.814	-160.4	3.336	65.9	0.025	87.4	0.706	-113.7
280	0.818	-161.7	3.227	63.2	0.027	91.3	0.716	-116.2
290	0.823	-164	3.1	61.1	0.029	95.1	0.722	-119.2
300	0.828	-165.4	2.986	58.9	0.032	97	0.724	-120
310	0.828	-166.3	2.935	57.3	0.035	98.2	0.726	-122.1
320	0.829	-168.2	2.879	54.3	0.038	97.5	0.735	-123.7
330	0.832	-169.5	2.71	50	0.04	96.9	0.743	-125.4
340	0.835	-170.9	2.536	46.9	0.042	97.3	0.747	-127.4
350	0.838	-171.9	2.395	45.7	0.044	97.7	0.756	-130
360	0.843	-173.6	2.266	44	0.045	98.3	0.761	-130.8
370	0.843	-174.9	2.117	43.2	0.048	100.3	0.767	-133.3
380	0.845	-175.5	2.027	42.7	0.051	100.7	0.772	-134.4
390	0.852	-176.8	1.986	43.3	0.055	101.6	0.779	-137
400	0.857	-178.2	1.969	42.8	0.059	102.6	0.788	-138.4
410	0.862	-178.9	1.938	41.7	0.062	101.6	0.793	-139.8
420	0.862	179.2	1.91	39.4	0.066	99.6	0.797	-141.6
430	0.861	178.7	1.895	37.1	0.068	98.7	0.801	-143.8
440	0.873	177.3	1.844	33.7	0.07	97.2	0.809	-145.3
450	0.868	176.3	1.73	30.5	0.072	96.9	0.814	-147
460	0.871	174.9	1.644	27.8	0.074	96.8	0.822	-148
470	0.875	175.2	1.558	26.8	0.077	97.3	0.821	-149.6
480	0.875	174.4	1.485	26.3	0.08	96.9	0.83	-150.6
490	0.878	172.8	1.394	25.7	0.083	97.1	0.829	-152.2
500	0.882	171.6	1.332	26.2	0.086	96.5	0.841	-153.6

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## D5001UK 175MHz TEST FIXTURE

**Substrate 1.6mm PTFE/glass,  $\epsilon_r = 2.5$**

**All microstrip lines  $W = 4.4\text{mm}$**

**T1 10mm**

**T2 13mm**

**T3 12mm**

**T4 4mm**

**L1 1.5 turns 22swg enamelled copper wire, 6mm id.**

**L2 10 turns 19swg enamelled copper wire, 6mm id.**

**L3 1.5 turns 22swg enamelled copper wire, 6mm id.**

**L4 13.5 turns 19swg enamelled copper wire on Siemens B64920A618x830 ferrite core**